

Notice of Allowability	Application No.	Applicant(s)		
	09/996,279	RISCH ET AL.		
	Examiner	Art Unit		
	Steven H. Rao	2814		
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The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.				
1. This communication is responsive to 6/30/04.				
2. The allowed claim(s) is/are <u>1-20</u> .				
3. The drawings filed on <u>28 November 2001</u> are accepted by the Examiner.				
 4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some* c) None of the: 1. Certified copies of the priority documents have been received. 				
2. Certified copies of the priority documents have been received in Application No				
3. Copies of the certified copies of the priority documents have been received in this national stage application from the				
International Bureau (PCT Rule 17.2(a)).				
* Certified copies not received:				
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.				
5. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.				
6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.				
(a) 🔲 including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached				
1) 🗌 hereto or 2) 🔲 to Paper No./Mail Date				
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date				
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).				
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.				
Attachment(s)				
1. Notice of References Cited (PTO-892)	5. Notice of Informal Pa	atent Application (PTC	D-152)	
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summary			
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0	Paper No./Mail Date 8), 7. ☐ Examiner's Amendm	Paper No./Mail Date 7. Examiner's Amendment/Comment		
Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit	8. ⊠ Examiner's Stateme	nt of Reasons for Allo	wance	
of Biological Material	9.			

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Response to Amendment

Applicants' amendment filed on June 30, 2004 ahs been entered.

Therefore claims 1-20 as recited in the amendment are currently pending in the Application.

Claims 21-25 have been cancelled.

Reasons for allowance

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitation of the dependent claims, in such manner that a rejection under 35 U.S.C. 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in independent claims, which include A method for fabricating a double gate MOSFET, which comprises the steps in the following sequence producing gate aligned accurately with one another by; providing a substrate structure having a silicon substrate layer, a first insulation layer disposed on the silicon substrate layer. a first separation layer disposed on the first insulation layer, and a semiconductor layer disposed on the first separation layer; patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET; depositing a second separation layer on the semiconductor layer structure and the first separation layer; completely embedding the semiconductor layer structure in the first and second separation layers by patterning the first and second separation layer on a structure

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formed of the first and second separation layers; vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between then, during the etching of the two depressions, the second insulation layer, the first and second separation layers and, in each case on both aides, an edge section of the semiconductor layer structure being etched through completely in each ease; filling the depression with a material; an electrically conductive forming a contact hole in the second insulation layer; removing a region of the separation layer extending from the contact hole to the semiconductor layer structure and in which region the semiconductor layer structure is embedded in the separation layers by etching the region of the separation layers through the contact hole; applying third insulation layers on inner walls of the region of removed separation layers and on surfaces of the semiconductor layer structure; and introducing a further electrically conductive material into the region of the removed separation layers. The Applicants' further state/ represent that the recited sequence of performing the steps results in the very accurate alignment of gate electrodes which has not hereto been achieved in the prior art. (applicants -remarks section- After Final amendment pages 16-17).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on weekdays between 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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